REMARKS/ARGUMENTS

In this amendment, claim 1 is amended; and no claims are canceled or added.

Drawings

Formal drawings for figures 1-16 are being submitted as attachments.

Allowed subject matter

Applicants note with appreciation the indicated allowability of claims 4, 5, 6, 11, and 13-20.

Claims 1-4

Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by the published article "High-Speed CRC Computation Using State-Space Transformations" by Derby, and under 35 U.S.C. 103(a) as being unpatentable over Weldon and Weldon in view of U.S. Patent No. 3,634,883 to Kreidermacher.

Claim 1 is allowable over the cited references, either alone or in combination, as those references fail to teach or suggest all the elements of claim 1. For example, claim 1 recites:

> *computing a plurality of feedforward bits for the first word by:*
> *logically combining message bits of K potentially overlapping groups of the N message bits to form K logical expressions, wherein K and N are integers, K is less than N, and each of the logical expressions consists of only message bits,*
> *combining the K logical expressions into a plurality of terms, and*
> *storing the plurality of terms as a plurality of feedforward bits;*

103 rejections

These rejections only address the "storing" claim element from above. *See Office Action*, paragraphs 5 and 6. Applicant respectfully requests an identification of where the combining steps occur in Weldon and Kreidermacher.

Note that in Weldon, multipliers 245 and 445 multiply respective bits of the message R by respective coefficients of the shift polynomial. *See Weldon*, col. 6 lines 49-63. The bits of the message R are not combined before this multiplication and before adders 230, particularly not into logical expressions that are then combined into terms. Thus, Weldon does

not teach or suggest combining message bits to form logical expressions and combining the expressions into terms, as recited in claim 1.

Kreidermacher is cited for providing a data register for a ROM in hardware logic. This teaching does not make up for the limitations of Weldon.

102 rejections

Derby transforms the CRC equations to form a matrix equation (5), (10). *See Derby*, page 167. This allows the matrix multiplications, e.g. equation (19), to be pipelined. *Id.*, page 169 left column. In the matrix multiplication, the sum of products of an input s(m) and coefficients of the matrix B are partitioned so that at each stage the contributions of two inputs are added. *Id.*, page 169 left column at bottom. These products thus contain coefficients of the matrix B. Moreover, the pipeline registers that receive the products also utilize these products. *Id.*, page 170, left column lines 16+. Thus, Derby does not teach or suggest wherein "*each of the logical expressions consists of only message bits,*" as recited in claim 1.

For at least these reasons, claim 1 is allowable over the cited references. As claim 1 is allowable, dependent claims 2-4 are also allowable for at least the same rationale.

Claims 7-12

Claims 7-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Weldon. Claims 7-9 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Derby.

Claim 7 is allowable over the cited references, either alone or in combination, as those references fail to teach or suggest all the elements of claim 7. For example, claim 7 recites:

> *the feedforward circuit receives message bits and provides an output to the logic circuit after N clock cycles, and the feedback circuit receives the cyclical redundancy check bits and provides an output to the logic circuit after 2N clock cycles.*

The Office Action appears to have not addressed this claim element. *See Office Action*, paragraphs 2 and 3.

In Weldon, the multipliers 245 (or 445) and the multipliers 240 (or 440) perform their operations in the same number of clock cycles. *Id.*, col. 6 lines 35-63. Thus, Weldon does not teach or suggest the above limitation.

In Derby, based on equations (5), (10), and (13), which are essentially the same, the feedforward circuit and the feedback circuit take the same number of clock cycles to provide an output. For example, each new cycle produces a new x(n+1) from the current cycle results of the A and B multiplications. Accordingly, Derby also does not teach or suggest the above limitation.

For at least these reasons, claim 7 is allowable over the cited references. As claim 7 is allowable, dependent claims 8-12 are also allowable for at least the same rationale.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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